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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:		§		
	Samson X. Huang	§	Art Unit:	2673
		§		
Serial No.:	09/846,065	§	Examiner:	Prabodh M. Dharia
		§		
Filed:	April 30, 2001	§	Conf. No.:	4510
		§		
For:	Reducing the Bias on Silicon Light Modulators	§ §	Atty Docket:	ITL.0563US P11334

Mail Stop **Appeal Brief-Patents**
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P.O. Box 1450
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APPEAL BRIEF

Date of Deposit: September 20, 2004
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Cynthia L. Hayden

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-11 are rejected. Each rejection is appealed.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Referring to Figure 1, a spatial light modulator 10 includes a liquid crystal layer 18. The liquid crystal layer 18 is sandwiched between a pixel electrode 20 and a transparent top plate 16. Applying voltages across the liquid crystal layer 18 through the top plate 16 and pixel electrode 20 allows the reflectivity of the spatial light modulator 10 to be altered. A glass layer 14 may be applied over the top plate 16.

A drive circuit 23 applies bias potentials 12 and 22 to the top plate 16 and pixel electrode 20 respectively. Referring to Figure 2, the drive signal 12 is applied to the top plate 16 and the drive signal 22 is applied to the pixel electrode 20. During a positive frame, a signal 12 of $-V_a$ is applied to the top plate 16. During the negative frame, a voltage of V_b is applied to the top plate 16. At the same time, the pixel electrode voltage 22 is applied. The voltage 22 reaches a peak equal to the voltage level b during the negative frame. The difference between the voltage level b and the voltage V_b is indicated as the voltage a.

Thus, to provide a hypothetical example, if a liquid crystal material 18 has a 3.3 volt modulation voltage. The level b is equal to 1.8 volts. In the positive frame, the top plate 16 is biased to -1.5 volts (i.e., $V_a = 1.5$ volts). In the negative frame, the top plate 16 may be biased to 3.3 volts (i.e., $V_b = 3.3$ volts).

Referring to Figure 3, which shows the positive frame, the dynamic range is equal to b volts. If the spatial light modulator's supply voltage is a voltage equal to or higher than b volts, full modulation may be achieved by biasing the top plate to $-V_a$ volts in the positive frame. By using a negative voltage to bias the top plate 16, the entire dynamic voltage range (b volts) may be utilized while enabling lower overall supply voltages to be utilized for modulation. Conventional designs may have negative frame voltage as high as the voltage a plus the voltage b. See specification at page 3, line 12 through page 5, line 2.

Because the liquid crystal material 18 should not generally be biased only in the positive direction to avoid damage, the liquid crystal bias direction is altered on alternating frames. In the negative frame, the top plate 16 voltage may be V_b as shown in Figure 4. The spatial light modulator voltage still swings between zero and b volts. The corresponding gray scale is also reversed. As a result, zero volts produces the highest brightness and b volts produces the lowest brightness, as shown in Figure 4.

Thus, leading edge semiconductor supply voltages may be utilized to bias liquid crystal materials that would otherwise require supply voltages beyond those available with ever decreasing leading edge semiconductor supply voltages. As a result, an effective liquid crystal device may be achieved using existing and future silicon technologies. This may facilitate the integration of silicon and display technologies. See specification at page 5, line 2 through page 5, line 19.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Are Claims 1-11 Obvious Over Johnson in View of McKnight?

ARGUMENT

A. Are Claims 1-11 Obvious Over Johnson in View of McKnight?

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,073,010 to Johnson et al. (hereinafter, "Johnson") in view of U.S. Patent No. 6,329,971 to McKnight. The method of claim 1 includes biasing a first plate of a spatial light modulator with alternating signals of a first polarity during a positive cycle of liquid crystal modulation and a second polarity during a negative cycle of liquid crystal modulation and biasing a second plate of the spatial light modulator with only the second polarity during both the positive and negative cycles of liquid crystal modulation.

Use of an opposite polarity during a particular color cycle with respect to the polarity used to bias the pixel electrode is not taught by the McKnight reference. For example, during a positive color cycle a positive voltage is applied to the cover class electrode and negative plurality voltage is applied during negative color cycle which is opposite to what is covered by claim 1. In other words, the same polarity during a negative cycle of the liquid crystal modulation is not used to bias the second plate during both the positive and negative cycles of the liquid crystal modulation in the McKnight reference. For example, in Figure 13, positive voltage is used during red positive cycle for biasing the cover glass electrode and a negative voltage is used during negative red cycle but the pixel electrode is biased at positive voltage as shown in Figure 11. Therefore, the same polarity, as used for the negative color cycle, is not used to bias the pixel electrode, as is the case in claim 1.

By using a negative voltage to bias the top plate 16, for example, during the positive frame, the entire dynamic voltage range may be utilized while enabling lower overall supply voltages to be utilized for modulation. For example, for a liquid crystal material having a modulation voltage of 3.3 volts, the dynamic range Vb of 1.8 volts may be realized. In the positive frame, the top plate 16 may be biased to -1.5 volts (i.e., Va equal to 1.5 volts). In the negative frame, the top plate 16 may be biased to 3.3 volts (i.e., Vb equal to 3.3 volts). If the spatial light modulator's supply voltage is a voltage equal to or higher than b volts, full modulation may be achieved by biasing the top plate 16 to –Va volts in the positive frame. In the negative frame, the top plate 16 voltage may be Vb. The spatial light modulator voltage still swings between 0 and b volts.

However, the display system taught by the McKnight reference can have a negative frame voltage as high as voltage Va plus voltage Vb because during the positive color cycle (sub frame) a positive voltage is applied to the cover glass electrode and during the negative color cycle (sub frame) a negative voltage is applied to the cover glass electrode and during both negative and positive color cycles (sub frames) a positive voltage is applied to the pixel electrode. Therefore, to bias the liquid crystal material in the McKnight reference, relatively higher supply voltage will be required but the supply voltage of modern silicon chips is moving downwardly from 2.5 volts towards 1.3 volts and potentially lower thereafter. Thus, because of this biasing scheme, the McKnight reference may not be suitable for integrated circuit chips, which may not have the sufficient voltage levels to modulate typical liquid crystal materials. As a result, the McKnight display system could not be integrated into silicon chips.

Therefore, the rejection of the claims should be reversed.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: 9/17/04

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CLAIMS APPENDIX

The claims on appeal are:

1. A method comprising:

biasing a first plate of a spatial light modulator with alternating signals of a first polarity during a positive cycle of liquid crystal modulation and a second polarity during a negative cycle of liquid crystal modulation; and

biasing a second plate of said spatial light modulator with only the second polarity during both the positive and negative cycles of liquid crystal modulation.

2. The method of claim 1 including biasing a top plate and a pixel electrode.

3. The method of claim 2 including biasing said top plate to a negative voltage.

4. The method of claim 3 including maintaining said pixel electrode at a positive voltage.

5. The method of claim 4 including biasing said pixel electrode across its full dynamic range.

6. The method of claim 1 including alternately biasing the top plate negatively and positively.

7. A spatial light modulator comprising:

a top plate;

a liquid crystal layer;

a pixel electrode, said top plate and said pixel electrode sandwiching said liquid crystal layer; and

a drive circuit to apply positive potential during a negative cycle of liquid crystal modulation and apply negative potential during a positive cycle of liquid crystal modulation to said top plate and to bias the pixel electrode with only a positive potential during both the positive and negative cycles of liquid crystal modulation.

8. The spatial light modulator of claim 7 including a drive circuit to apply a negative bias potential to said top plate.

9. The spatial modulator of claim 7 wherein said spatial light modulator is a liquid crystal over silicon spatial light modulator.

10. The spatial light modulator of claim 7 wherein said drive circuit applies positive and negative bias potentials in alternating frames.

11. The spatial light modulator of claim 8 wherein said top plate is formed of indium tin oxide.

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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
ITL.0563US

In Re Application Of: **Samson X. Huang**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/846,065	**April 30, 2001**	**Prabodh M. Dharia**	**21906**	**2673**	**4510**

Invention: **Reducing the Bias on Silicon Light Modulators**

COMMISSIONER FOR PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **August 19, 2004**

The fee for filing this Appeal Brief is: **$330.00**

☒ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**

Signature

Dated: **September 20, 2004**

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I certify that this document and fee is being deposited on **09-20-2004** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Signature of Person Mailing Correspondence

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